Relevance of Analog -Today's SoC World

"An Overview of Analog & Mixed-Signal Design in deep sub-7nm Technology"

The paradigm shift of semiconductor industry from Analog based design to digital designs with higher transistor density was predicted around the early 21st century. With such growth, it was also predicted that the Analog would be ceased out and digital will be the design choice for an SoC.

Currently, as transistor technologies are shrinking below 7nm, the requirement for faster interfaces with high-speeds (such 112 Gbps or more) has become very much essential. Designing such high-speed interfaces are very much challenging in digital domain, as the supply voltage is scaled down with tightened power constraints in advanced technologies. These factors challenge the usage of pure digital design circuitry for e.g. I/O, PLL, DLL etc with the constraints mentioned above in an SoC design.

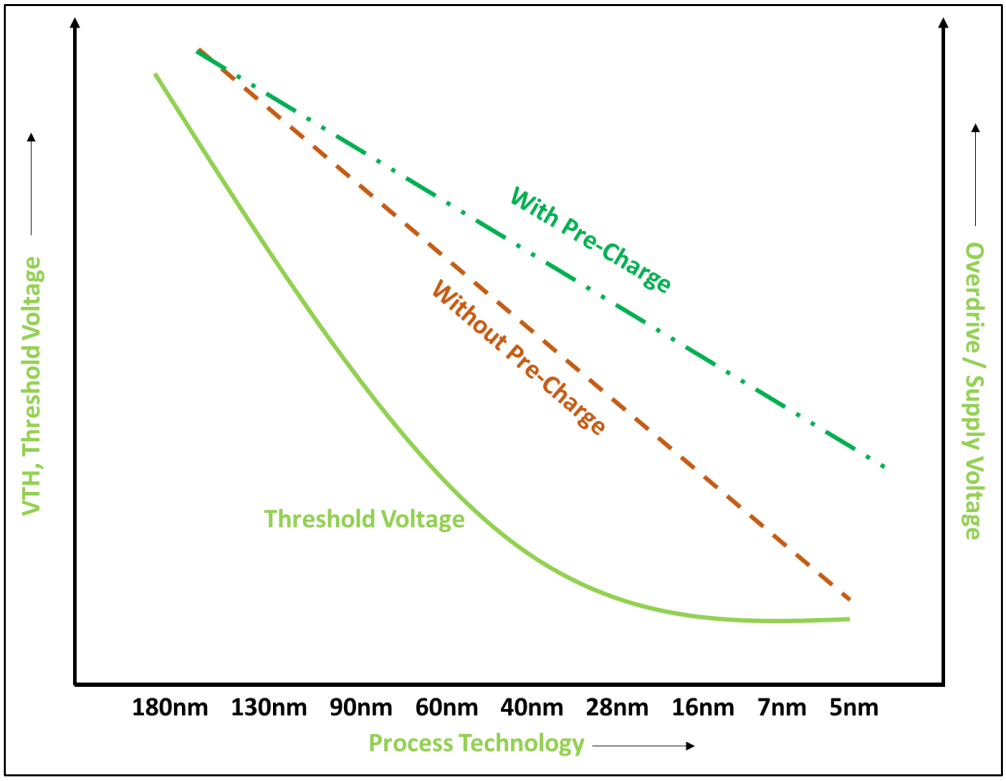
Emerging applications like Artificial Intelligence (AI), High-Performance Computing (HPC), High-Speed Networking etc., multi-cross functional features are added in SoCs. For implementing such features, designers are leveraging optimization techniques in RTL logic, standard cell design, physical design, complex DRC rules and double patterning methods. But these optimizations techniques hit the wall when it comes to I/O design. Therefore, there is a big need for Advanced Analog/ Mixed Signal design techniques in the Industry.

Striking the Right Balance: Analog & Digital

The earlier prediction of signal processing of sound, light, temperature, position, heartbeat etc. being only Analog driven and the others being digital is no more valid in the current day scenario. This is because of the strict narrow band restrictions mentioned in the specification, as there is an increase in the order of f_{op} (operating frequency). Therefore, many applications prefer Analog on Top designs rather than Digital on Top. The advanced interfaces like HBM, LPDDR, High-Speed D2D SerDes etc. has Analog on Top designs. Hence, there must be a strike between Analog and Digital before a design specification is fixed based upon the requirement and implementation.

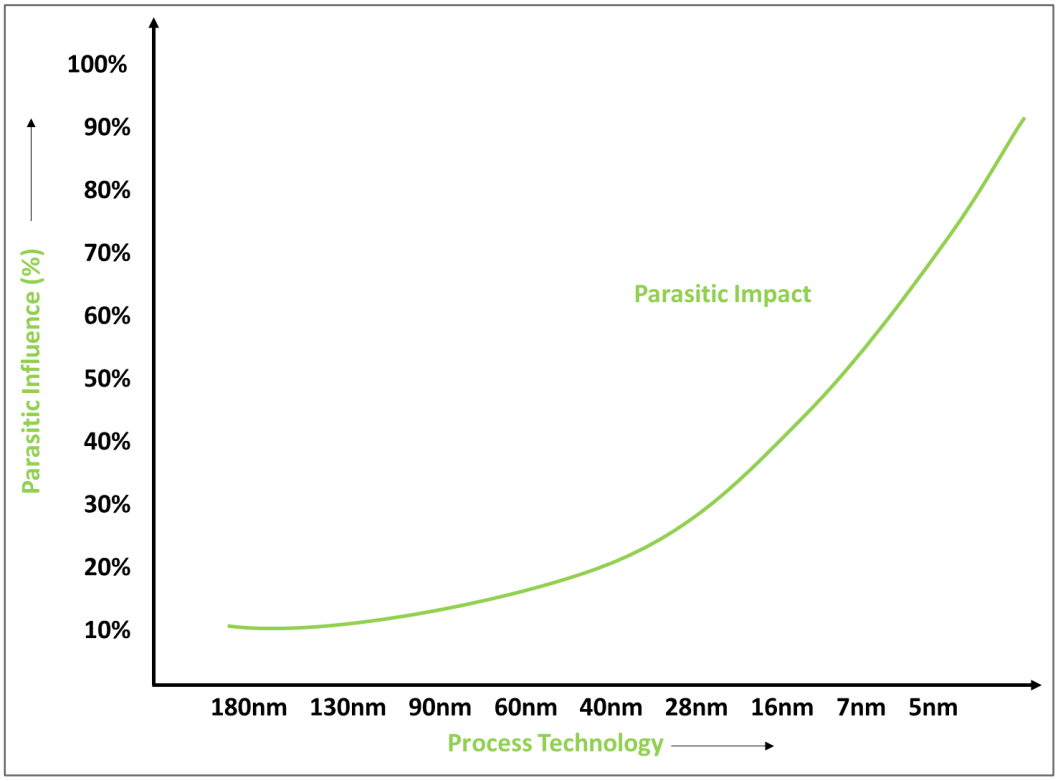
Analog Design sub-7nm technology: Critical Issues & Solution

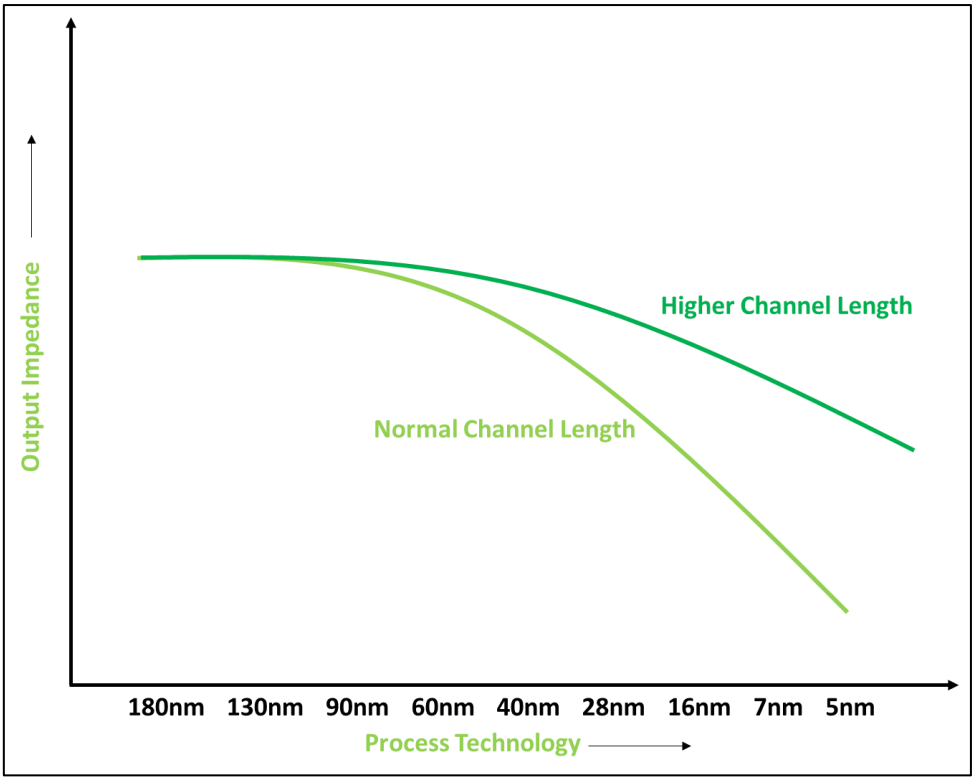
1. **Lower Supply Voltage**
   As channel lengths are shrinking, supply voltage is scaled down from 3.3 V to 0.7 V and is expected to go down further. This imposes lower overdrive issue for transistor (for both digital & Analog). This is overcome in Analog designs with the implementation of pre-charge nodes with initial conditions defined and make the design work in low overdrive.

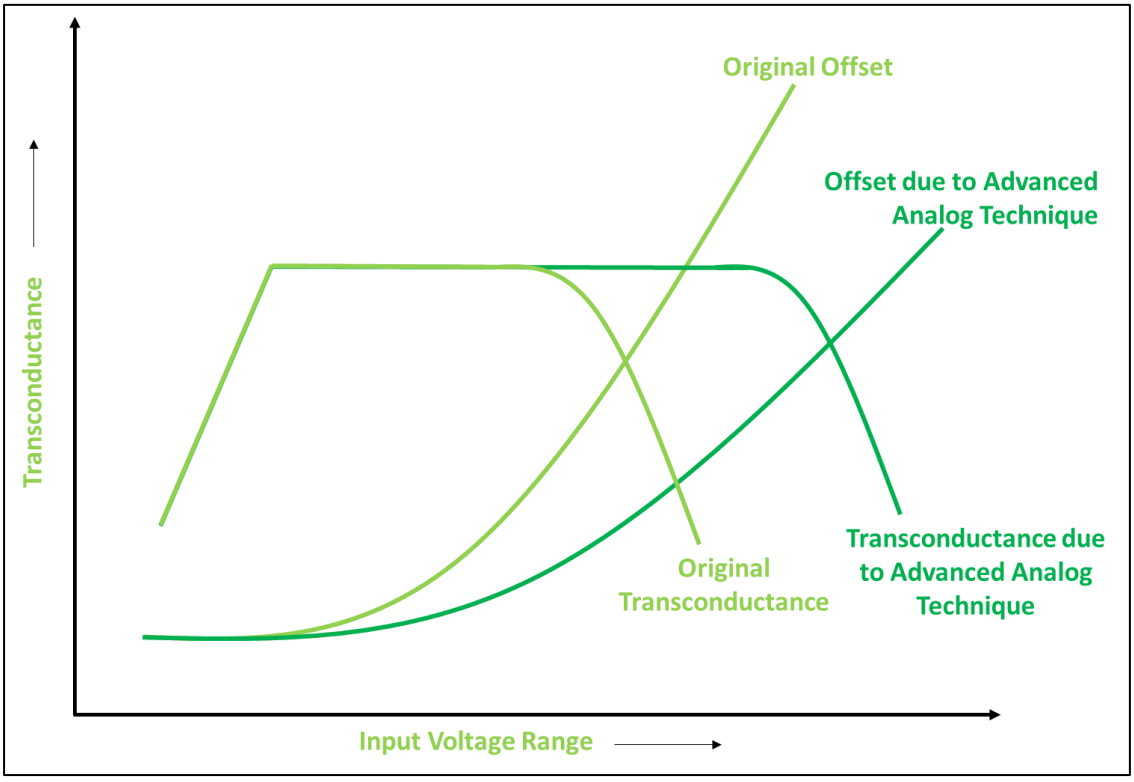


2. **Varying Transconductance**

Trans conductance is not constant over range of voltages and Offset becomes critical solution as the channel length scales down. In Analog design, this is issue is resolved by using higher channel lengths with significant VDS (~3X overdrive). This is not possible in digital designs, as we use auto minimum length usage (automation).

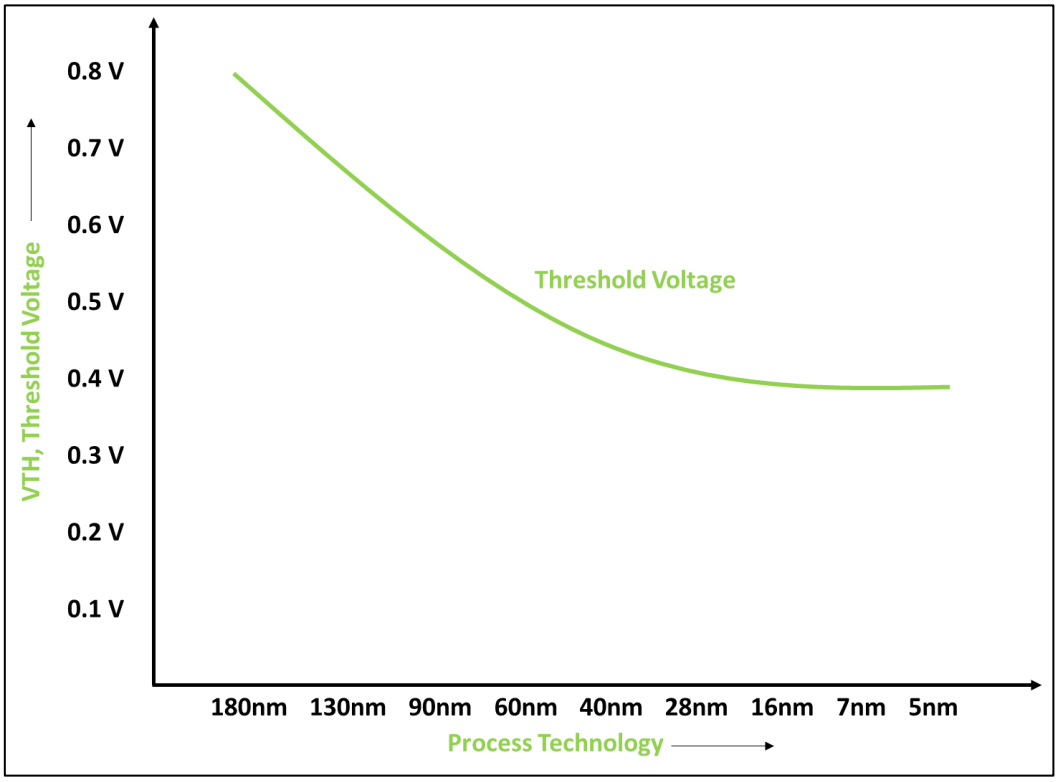






3. **High Threshold Voltages**
   In comparison to older technology nodes, threshold voltage (VTH) are nearing 50% of supply voltage (older nodes ~20%). This increase in threshold voltage w.r.t supply voltage is very challenging in terms of circuit design, as with available few mV, design is expected to work at

very high-speeds. To overcome the effect of higher threshold voltages, analog based designs uses pull-up and pull-down transistors.



Implementation Challenges & Strategies for sub-7nm Technology Designs

Digital Implementation Challenges

1. Digital implementation is based on scripts & automation. The script enhancements are not quite often, and the same script is used for a longer period. Individualistic knowledge of a script owner plays a key role in the automation flow.
2. Achieving smaller skew remains quite a challenge in digital, especially skews of 50 ps is highly impossible goal and it is a common required target for high-speed SoC designs of 4 Gbps & above.
3. EM/IR issues in digital are based on script quality. To improve IR drop and/or EM issues, automation expertise besides domain based expertise is a must.
4. In digital, the focus is more on APR tools, as the requirement of best and optimized Floorplan, Routing and Power Mesh Structures are very essential.

Advanced Analog Implementation Strategies

1. Pre-charge method for enabling advanced on-chip architectures to use ‘initial conditions’ for achieving higher performance.
2. Custom layout for parasitic matching helps in easy skew/ jitter targets for physical design and timing closure.
3. Accurate simulator or system level SI/PI sign-off for a complete 2.5D SiP
4. Accurate correlation between implementation and sign-off, thereby resulting in faster design convergence.
5. Accurate predictability on path delays, crosstalk and wire delays.

Analog and Mixed Signal - Design Challenges & Support

The transistors at sub-7nm technology increases the functional density, but when it comes to designing Analog circuits, the process is complex. Such small transistors withstand smaller supply voltage of up to 1 V. The requirement for operating Analog circuits is +/- 5 V (in older nodes) which is scaled down to: (i) 3.3 V (ii) 1.8 V (iii) 1.2 V (iv) 0.75 V; and is expected to scale down further for sub-7nm technology in coming days with the futuristic prediction of 0.5 V or even 0.2 V. Such reduction in supply voltage not only impact Analog circuits, but it also reduces the energy consumption of digital designs. However, the reduction in supply voltage for Analog circuits increases its susceptibility to noise/interference and degrades signal quality. Furthermore, the mismatches due to smaller transistors leads to random offset error, more flicker noise (1/f) and poor gain performance.

Digital & Analog handshake – A must

As wires/mm is increasing day-by-day in an ASIC, all the existing architectures and design techniques cease to work and there is a requirement of new ideas for design implementation like pre-charging of nodes for achieving higher speed, custom design/layout for crosstalk avoidance etc.

Advanced technology scaling offers new avenues for designing Analog circuits. In nanoscale processes, transistors will be unable to handle large voltages, but intrinsically switch very fast. This allows the designer to introduce different signal representations for Analog functions at the transistor level. Instead of using the traditional voltages or currents, time delays are used to represent Analog information. This opens a whole range of opportunities to explore newer circuits.

Also, with advanced technology, switching happens faster even when processing Analog information. In fact, Analog circuits are being built out of what traditionally are digital blocks, like switches or ring oscillators.

Industrial adoption of Analog yet again!

The Analog electronics field is going through a very exciting time. The digital revolution in electronics has made Analog even more necessary. Mobile devices are packed with Analog interfaces and Analog sensors, whose count increases with each new generation of the product. The Internet of Things (IoT) applications require lot of sensors (Analog & digital) for data collection and processing with constraints of power consumption and cost. Addressing such complex constraints by Analog designers opens a plenty of opportunities to make an impact in the Industry with ongoing revolution.

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